Attorney Docket No. 108298533US1 Disclosure No. 99-1116.01

In the Specification:

Please add a new section directly before the "Technical Field" on page 1 as follows:

CROSS REFERENCE TO RELATED APPLICATION

This	applica	ition is a div	risional ap	plication of U	nited St	ates Pater	٦t
Application	No.	09/641,498	entitled	"METHODS	FOR	FINISHIN	G
MICROELE	CTRON	IC DEVICE F	ACKAGES	S," filed on Au	gust 18,	2000, no	W
Patent No.		, which	is hereb	y incorporated	by refe	rence in it	s
entirety.	•					,	

Please amend the first full paragraph on page § (lines 7-18) as follows:

AB 7/26107

Figure 1 is an isometric view of a plurality of packaged microelectronic devices 100 before being processed in accordance with an embodiment of the invention. The microelectronic devices 100 can each have a microelectronic die 102, a printed circuit substrate 103 or lead frame to which each die 102 is attached, and a protective casing 110 covering each die 102. The dies 102 can be memory devices or processors that include integrated circuitry in a semiconductor substrate, or the dies 102 can be other types of microelectronic components. The printed circuit substrates 103 can each have a plurality of ball-pads 104 and traces 105 extending from the ball-pads 104. The traces 105 are coupled to corresponding bond-pads (not shown) on the die 102. The printed circuit substrates 103 shown in Figure 1 are initially part of an interposing substrate assembly 106, which may remain intact during the abrasion processes discussed below (as is evident in Figures 3-5). During Back-End-of-Line (BEOL) processing, the interposing substrate assembly 106 is cut to separate individual packaged devices 100 from one another.